AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of propagating signals on programmable interconnect in a programmable logic device, the method comprising:

selecting by a selection device between source signals to drive a shared programmable interconnect portion located on the programmable logic device; and

coordinating latching of the source signals in corresponding capture devices via a time multiplexing signal generator coupled to the selection device and the capture devices via one time multiplexing signal.

2. (Original) The method of Claim 1, wherein the source signals are provided by a configurable logic block in the programmable logic device.

3. (Original) The method of Claim 1, wherein the source signals are provided by configurable logic blocks in the programmable logic device.

4. (Previously Presented) The method of Claim 1, wherein the capture devices are provided in a configurable logic block in the programmable logic device.

5. (Previously Presented) The method of Claim 1, wherein the capture devices are provided in configurable logic blocks in the programmable logic device.

Claims 6-7. (Cancelled).

8. (Currently Amended) The ~~system~~ method of Claim 1, wherein the capture devices comprise latches.

9. (Previously Presented) The method of Claim 1 further comprising:

connecting the selecting device to the capture devices using a programmable interconnect point.

10. (Currently Amended) A method of propagating signals in a programmable logic device, the method comprising:

selecting by a selection device between source signals to route signals onto a shared programmable interconnect on the programmable logic device;

routing signals from the shared programmable interconnect to the capture devices through a first programmable interconnect point; and

controlling by a clock applied to the selection device and capture devices the provision of the source signals through the selection device [[and]] to the capture devices, wherein a first one of the signals is latched to a first one of the capture devices during a first phase of the time multiplexing signal and a second one of the signals is latched to a second one of the capture devices during a second phase of the time multiplexing signal.

11. (Previously Presented) The system of Claim 10, wherein the capture devices comprise latches.

12. (Previously Presented) The method of Claim 10, wherein additional programmable interconnect points connect the first programmable interconnect point to the capture devices.

13. (Currently Amended) A configured programmable logic device comprising:

a multiplexer which chooses between source signals to drive a shared programmable interconnect on the programmable logic device;

flip flops which receive the source signals from the shared programmable interconnect; and

a clock which is coupled to the multiplexer and flip flops and provides one of the source signals from the multiplexer to one or more of the flip flops without a clock delay.

14. (Previously Presented) The method of Claim 13, wherein the multiplexer is connected to the flip flops by a first programmable interconnect point.

15. (Previously Presented) The method of Claim 14, wherein additional programmable interconnect points connect the first programmable interconnect point to the flip flops.

16. (New) The method of Claim 1, wherein coordinating latching further comprises:

latching a first one of the source signals to a first capture device during a first phase of the time multiplexing signal; and

latching a second one of the source signals to a second capture device during a second phase of the time multiplexing signal.

17. (New) The method of Claim 1, further comprising receiving by each capture device of the time multiplexing signal on a D input terminal of the capture device.

18. (New) The method of Claim 1, further comprising:

receiving by a first one of the capture devices the time multiplexing signal; and

receiving by a second one of the capture devices an inversion of the time multiplexing signal.

19. (New) The method of Claim 1, wherein the time multiplexing signal generator comprises one of a single A/B switch signal, a multi-bit bus and a simple clock signal with a global reset signal indicating a first phase to synchronize the sources.

20. (New) The method of Claim 1, wherein the one time multiplexing signal comprises a single frequency signal.

21. (New) The method of Claim 13, further comprising:

receiving by a first one of more of the flip flops the one of the source signals; and

receiving by a second one or more of the flip flops an inversion of the one of the source signals.

22. (New) The method of Claim 13, wherein the clock signal comprises a single frequency signal.